

CP 2815

Atty. Dkt. No. 039153-0223 (E0554)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yu

Title: MOS TRANSISTOR WITH
ASYMMETRICAL
SOURCE/DRAIN EXTENSIONS

Appl. No.: 09/476,961

Filing Date: 01/03/2000

Examiner: Warren, M.

Art Unit: 2815

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| CERTIFICATE OF MAILING I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on the date below. <u>Joseph N. Ziebert</u> (Printed Name) <u>Joseph M. Ziebert</u> (Signature) <u>12-13-01</u> (Date of Deposit) |
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AMENDMENT TRANSMITTAL

Commissioner for Patents
Box NON-FEE AMENDMENT
Washington, D.C. 20231

Sir:

Transmitted herewith is Amendment A in the above-identified application.

- [] Small Entity status under 37 C.F.R. § 1.9 and § 1.27 has been established by a Small Entity statement previously submitted.
- [] Small Entity statement is enclosed.
- [X] The fee required for additional claims is calculated below:

| | Claims as Amended | | Previously Paid For | | Extra Claims Present | | Rate | | Additional Claims Fee |
|--|-------------------------|---|------------------------|---|----------------------------|---|----------|---|--------------------------|
| Total Claims: | 20 | — | 20 | = | 0 | x | \$18.00 | = | \$0.00 |
| Independents: | 3 | — | 3 | = | 0 | x | \$80.00 | = | \$0.00 |
| First presentation of any Multiple Dependent Claims: | | | | | | + | \$270.00 | = | \$0.00 |
| CLAIMS FEE TOTAL: | | | | | | | | | \$0.00 |

- [] Applicant hereby petitions for an extension of time under 37 C.F.R. § 1.136(a) for the total number of months checked below:

| | | | |
|--------------------------|---|------------|--------|
| <input type="checkbox"/> | Extension for response filed within the first month: | \$110.00 | \$0.00 |
| <input type="checkbox"/> | Extension for response filed within the second month: | \$390.00 | \$0.00 |
| <input type="checkbox"/> | Extension for response filed within the third month: | \$890.00 | \$0.00 |
| <input type="checkbox"/> | Extension for response filed within the fourth month: | \$1,390.00 | \$0.00 |
| <input type="checkbox"/> | Extension for response filed within the fifth month: | \$1,890.00 | \$0.00 |
| | EXTENSION FEE TOTAL: | | \$0.00 |
| | CLAIMS AND EXTENSION FEE TOTAL: | | \$0.00 |
| <input type="checkbox"/> | Small Entity Fees Apply (subtract ½ of above): | | \$0.00 |
| | TOTAL FEE: | | \$0.00 |

- ☐ Please charge Deposit Account No. 06-1447 in the amount of \$0.00 . A duplicate copy of this transmittal is enclosed.
- ☐ A check in the amount of \$0.00 is enclosed.
- ☒ The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.


Respectfully submitted,

Date

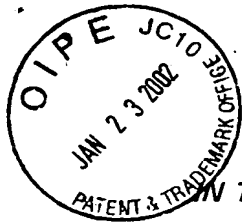
12-13-01

FOLEY & LARDNER
Firststar Center
777 East Wisconsin Avenue
Milwaukee, Wisconsin 53202-5367
Telephone: (414) 297-5768
Facsimile: (414) 297-4900

By



Joseph N. Ziebert
Attorney for Applicant
Registration No. 35,421



Atty. Dkt. No. 039153-0223 (E0554)

7/8 Churisa
2-15-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yu

Title: MOS TRANSISTOR WITH
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AMENDMENT

Commissioner for Patents
Box NON-FEE AMENDMENT
Washington, D.C. 20231

Sir:

This communication is responsive to the Office Action dated September 13, 2001, concerning the above-referenced patent application.

Please amend the application as follows:

IN THE CLAIMS:

In accordance with 37 C.F.R. § 1.121, please substitute for original claims 31, 32, 36, and 37 the following rewritten versions of the same claims, as amended. The changes are shown explicitly in the attached "Version with Markings to Show Changes Made".

- C*
B
- 1 31. (Once Amended) An ultra-large scale integrated circuit including a
 - 2 plurality of field effect transistors, the field effect transistors comprising:
 - 3 a gate structure on a top surface of a semiconductor substrate;
 - 4 a source extension with dopants of a first conductivity type;
 - 5 a drain extension with dopants of the first conductivity type; and